

General Features

- Proprietary New Super-Junction Technology
- $R_{DS(ON),typ.}=56m\Omega@V_{GS}=10V$
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode
- Lead Free Package and Finish

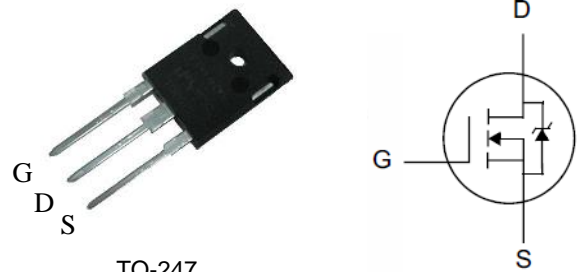
Applications

- Adaptor
- Charger
- SMPS Standby Power
- Switching Voltage Regulators

BV_{DSS}	$R_{DS(ON),typ.}$	I_D
650V	56m Ω	48A

Ordering Information

Part Number	Package	Brand
CN48N60M2	TO-247	ChipNobo



TO-247

Package Not to Scale

Absolute Maximum Ratings

 $T_c=25^{\circ}C$ unless otherwise specified

Symbol	Parameter	Value	Unit
		CN48N60M2	
V_{DSS}	Drain-to-Source Voltage ^[1]	650	V
V_{GSS}	Gate source voltage (static)	± 30	
I_D	Continuous Drain Current @ $T_c = 25^{\circ}C$	48	A
	Continuous Drain Current @ $T_c = 100^{\circ}C$	31	
I_{DM}	Pulsed Drain Current at $V_{GS}=10V$	178	
E_{AS}	Single Pulse Avalanche Energy $L=10mH$	550	mJ
P_D	Power Dissipation	431	W
dv/dt	Drain Source voltage slope, $V_{DS} \leq 480V$	50	V/ns
dv/dt	Reverse diode dv/dt, $V_{DS} \leq 480V, I_{SD} < I_D$	50	V/ns
T_J & T_{STG}	Operating and Storage Temperature Range	-55 to 150	$^{\circ}C$

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	Max. Value	Unit
		CN48N60M2	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.29	$^{\circ}C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	50	

Electrical Characteristics

OFF Characteristics

 $T_J = 25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	650	--	--	V	$V_{GS}=0V, I_D=250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	--	--	5	μA	$V_{DS}=650V, V_{GS}=0V$
		--	--	200		$V_{DS}=520V, V_{GS}=0V, T_J=125^\circ\text{C}$
I_{GSS}	Gate-to-Source Leakage Current	--	--	+100	nA	$V_{GS}=+30V, V_{DS}=0V$
		--	--	-100		$V_{GS}=-30V, V_{DS}=0V$

ON Characteristics

 $T_J = 25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	--	56	68	$m\Omega$	$V_{GS}=10V, I_D=20A$
$V_{GS(TH)}$	Gate Threshold Voltage	2.5	--	4.5	V	$V_{DS}=V_{GS}, I_D=250\mu A$

Dynamic Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{iss}	Input Capacitance	--	3465	--	pF	$V_{GS}=0V, V_{DS}=50V, f=1.0MHz$
C_{oss}	Output Capacitance	--	99.5	--		
C_{riss}	Reverse Transfer Capacitance	--	6.5	--		
Q_g	Total Gate Charge	--	77	--	nC	$V_{DD}=300V, I_D=20A, V_{GS}=0 \text{ to } 10V$
Q_{gs}	Gate-to-Source Charge	--	17	--		
Q_{gd}	Gate-to-Drain (Miller) Charge	--	30.5	--		

Resistive Switching Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	25	--	ns	$V_{DD}=300V, I_D=20A, V_{GS}=10V, R_g=2.35\Omega$
t_{rise}	Rise Time	--	23	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	56	--		
t_{fall}	Fall Time	--	28	--		

Source-Drain Body Diode Characteristics
 $T_J=25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min	Typ.	Max.	Unit	Test Conditions
I_{SD}	Continuous Source Current ^[2]	--	--	48	A	Maximum Ratings
I_{SM}	Pulsed Source Current ^[2]	--	--	178		
V_{SD}	Diode Forward Voltage	--	--	1.2	V	$I_S=20\text{A}$, $V_{GS}=0\text{V}$
T_{rr}	Reverse Recovery Time	--	180	--	ns	$I_S=20\text{A}$, $di/dt = 100\text{A/us}$
Q_{rr}	Reverse Recovery Charge	--	965	--	nC	

Note:

[1] $T_J=+25^{\circ}\text{C}$ to $+150^{\circ}\text{C}$

[2] Pulse width $\leq 380\mu\text{s}$; duty cycle $\leq 2\%$.

Typical Characteristics:

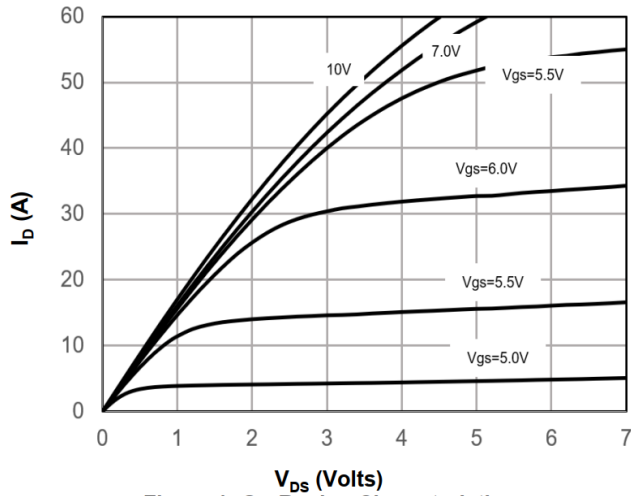


Figure 1: On-Region Characteristics

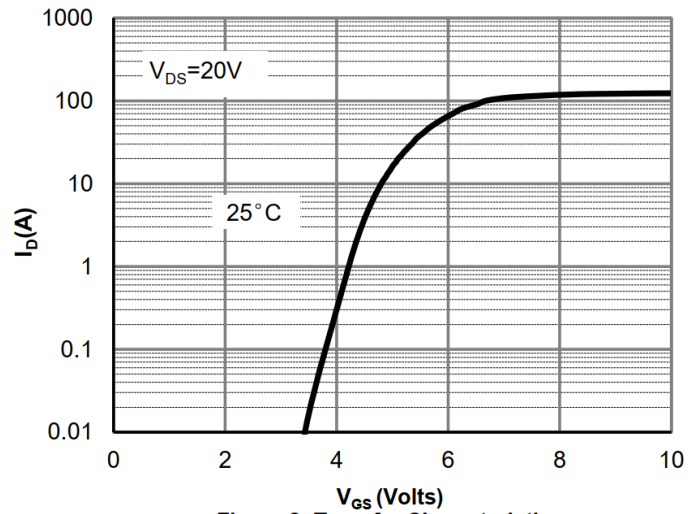


Figure 2: Transfer Characteristics

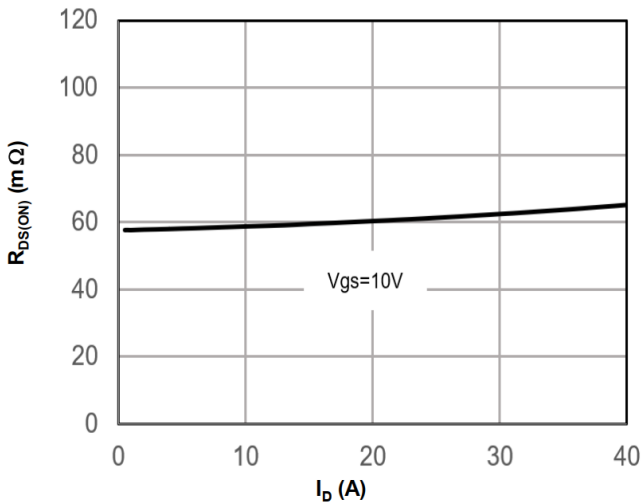


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

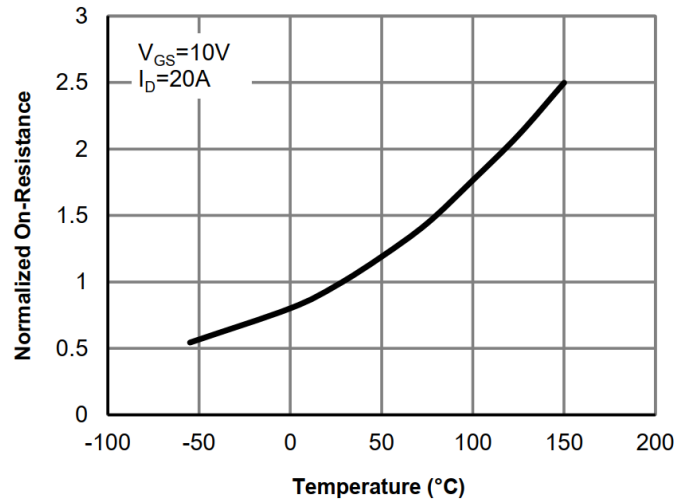


Figure 4: On-Resistance vs. Junction Temperature

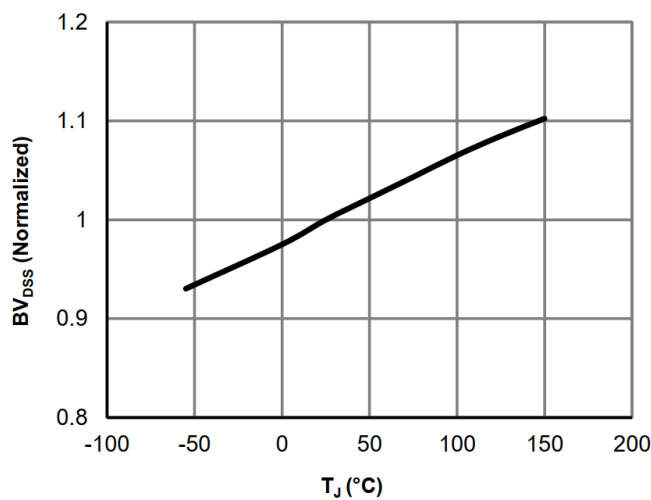


Figure 5: Break Down vs. Junction Temperature

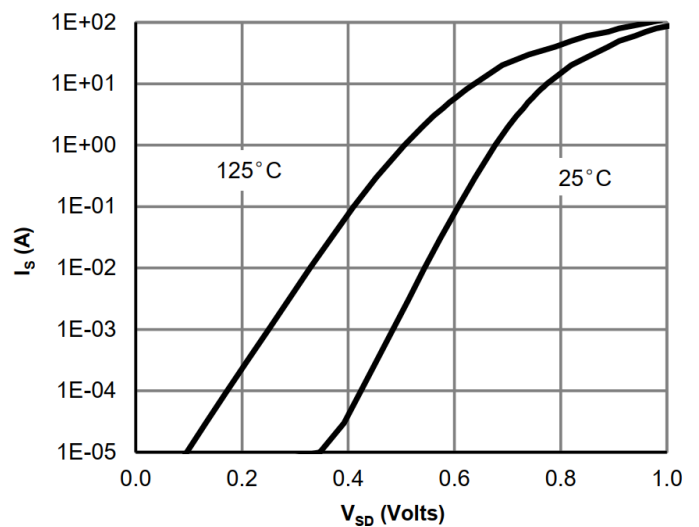


Figure 6: Body-Diode Characteristics

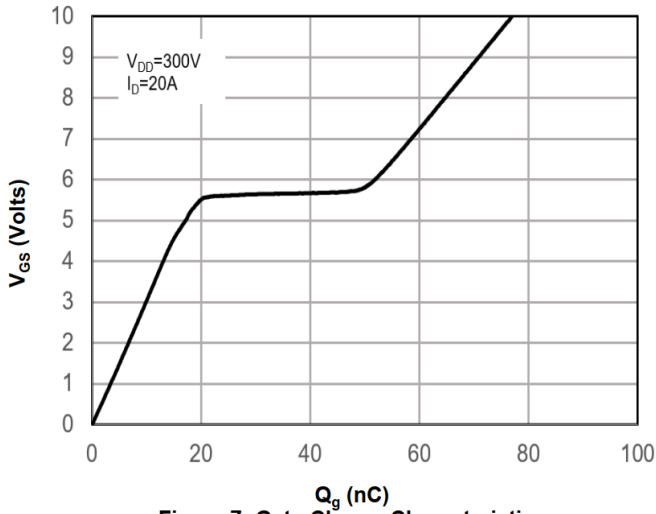


Figure 7: Gate-Charge Characteristics

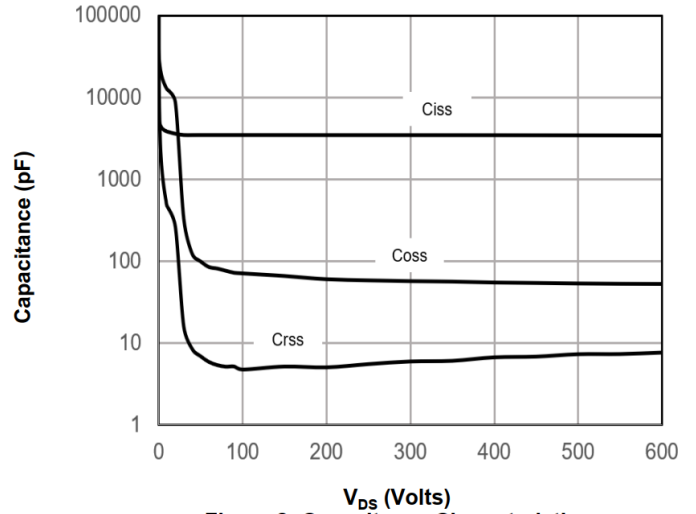


Figure 8: Capacitance Characteristics

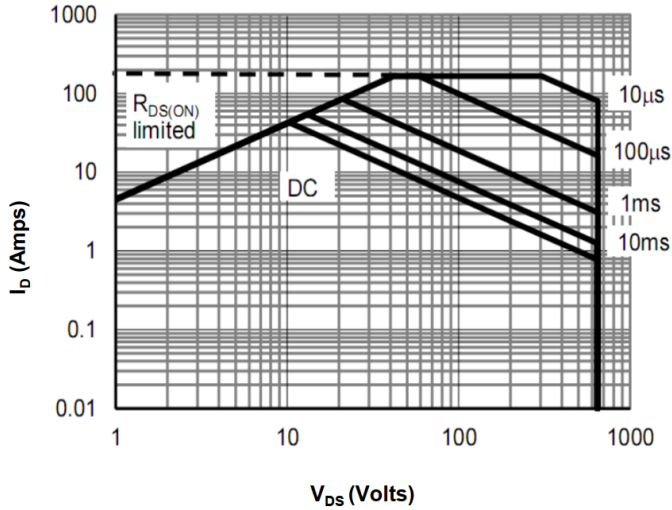


Figure 9: Maximum Forward Biased Safe Operating Area

Test Circuits and Waveforms

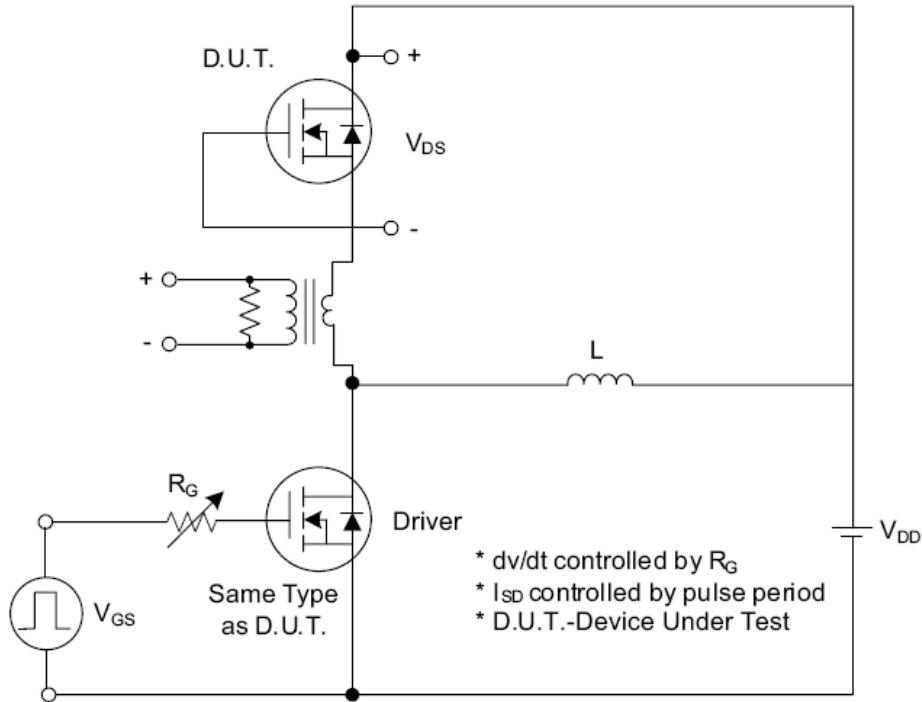


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

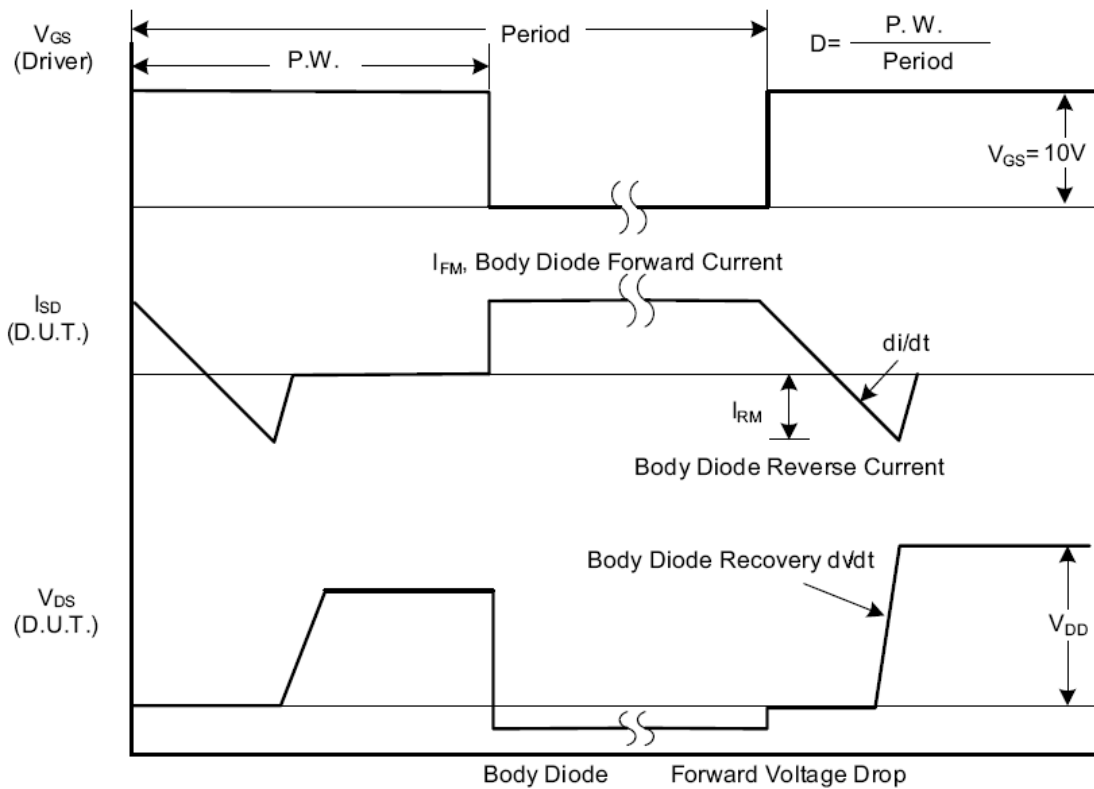


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

Test Circuits and Waveforms (Cont.)

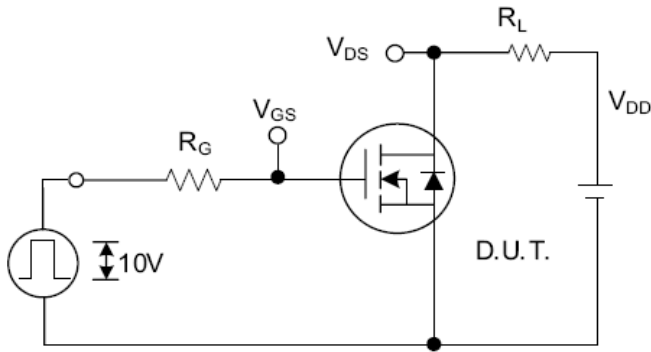


Fig. 2.1 Switching Test Circuit

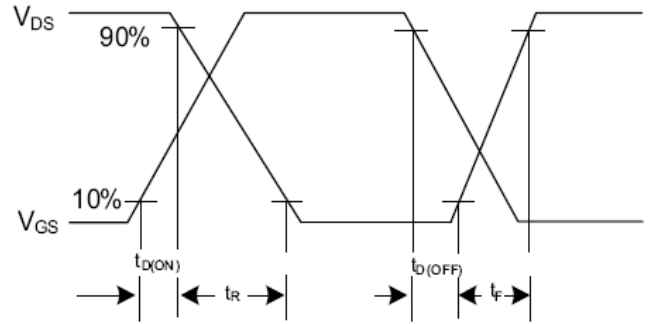


Fig. 2.2 Switching Waveforms

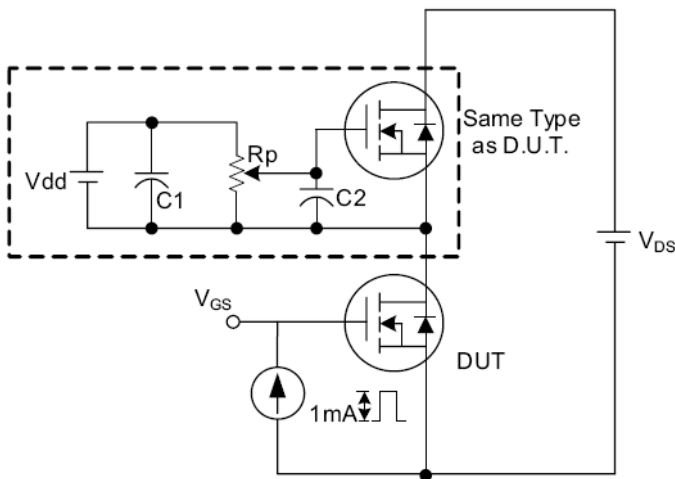


Fig. 3.1 Gate Charge Test Circuit

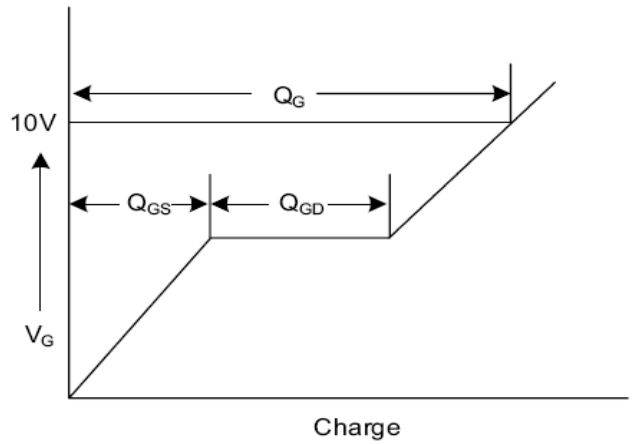


Fig. 3.2 Gate Charge Waveform

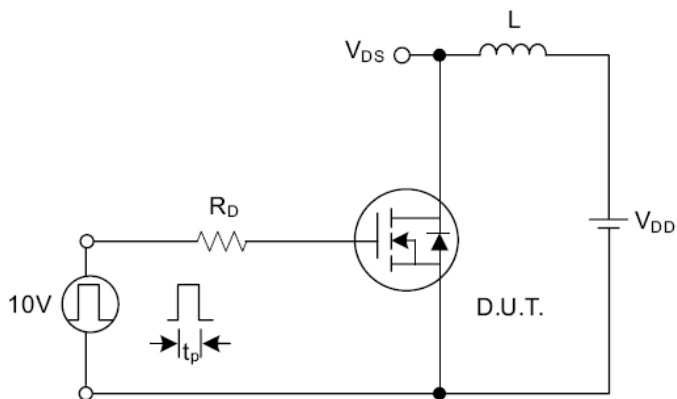


Fig. 4.1 Unclamped Inductive Switching Test Circuit

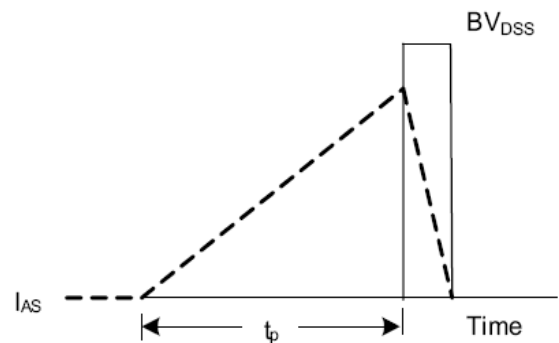


Fig. 4.2 Unclamped Inductive Switching Waveforms

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